June 2001

Processors

of Network Services

Introducing the CNP810 Family
- 3rd Party Tools
- Reference Board
- SDK
- CPNP810SP Overview
- Product Overview
- Network Services Processors
- Company Overview

Agenda
partners for total solutions

Announcing reference design hardware

chain & 3rd party partners

Announcing comprehensive development tool

unveiling new company name

services processor

unveiling first product - CNP810SP network

What are we announcing?
Multithreading (SMT)

- Storage systems
- Edge routers
- Shapers
- Web switches and traffic

For use in

Interface (runs MIPS code)

Standard programming
(25 MP/s)

Higher performance services (NSP)

Clearwater Networks: Overview
Ankur Shah
- Partner, Goldman Sachs
- Hughes LAN Systems
- Founding CEO of Rapid City, CEO of
- Former VP, Nortel Networks
- CEO of Plunks

Joe Kennedy
- Technology
- Founding CEO of S3, Chips &
- Managing Partner, Tailwood Ventures

Dado Banatao
- Former CTO of Natl Semi!
- Extreme Networks Director
- CEO of Adaptive Silicon

Charles Cнимalli
- General Partner, Mayfield Funds
- Kevin Fong

Ventures (Dado Banatao)
- Mayfield Led, also Tailwood
- $50M total
- July 1999
- Series A funding closed

- Maintained pro rata
- Mayfield and Tailwood
- Synopsys, others
- Mitsuji, Sands Bros.,
- Goldman Sachs Led, also
- $30M total
- Jan 2001
- Series B funding closed

Fundings Status & Outside Directors
Management Team

- Nexgen
  - Director of Hardware
    - Korbijn Vandyke
  - National Semiconductors
    - Joe Salvador, Director
- Selectica
  - HR
    - Diane Jacobson, VP of
      - C-Cube Engineering
    - Brad Howe, VP of
      - Araereal Semiconductor
- Operations
  - Murty Cheruvu - VP of
    - Semiconductor
  - National
    - Ron Bar, Director of Corporate Development
    - Dan O'Neill, President CEO
Emergence of Network Services
- 1 per box
- Most often MIPS core CPU
- Exceptions/Services handled in Control Plane
  - 1 NP per blade => 8-16 nps per box
  - Examples: Intel IXP1200, C-Port C-5, IBM NP4G53
- Often proprietary ISA's for forwarding engines
- Forwarding
  - Focus on ASIC replacement for L2/3 fast path

Network Processors: First Wave
- 2001: New IETF RFC's = 84 (through April)
- 2000: New IETF RFC's = 281
- 1999: New IETF RFC's = 57

- cpq:

Increasing rate of change demands flexibility of

- MPLS, QoS, Load Balancing, Traffic Shaping,
- Billing, Intrusion Detection, Firewall, VPN, IPsec,
- Generation networking equipment

Adoption of value-added services is driving next

Emerging Network Services
technology change

Business models are driving

The Need for Services
Functional Integration of Network Services

The Need for Services
Packets per second

Instructions per packet

Implementations
Suitable for SOC
- Cycles
- Manage development
- Investment
- Leverage existing compatibility
- Maintain code
- Scalable
- Mask memory latency
- exploited parallelism
- Performance

Needed: Network Services Processor

Today's solutions are inadequate
- Will move to line cards
- Initially on service cards
- Services processors to handle
- Shift to distributed
- Bottleneck
- CPU has become system
- As services grow, control
- handled by Control CPU
- Originally, services

Emerging Services Bottleneck

NETWORKS
CLEARWATER
- High packet throughput + high CPU performance
- Good tools
- Simple programming model

Requirements:

- 1 NSP per blade => 8-16 nsp's per box
- Line card: NSP focused on exception processing
- Services card: NSP processes all packets sent to
- Focus on higher layer processing

The Next Wave

Network Services Processors:
The Road Blocks
Memory Latency:

- Memory Accesses Increasing
- Minimal Locality of Reference
- Large State Tables
- Poor Cache Utilization
- The Limiting Factor for CPU

Memory Latency in Cycles

Processors clock speeds worsen with increased MIPS processors end up stalled for long periods of time.
<table>
<thead>
<tr>
<th>Simple Programming Model</th>
<th>Multi-Threading (SIMT (Simultaneous Multithreading))</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hides Memory Latency</td>
<td>Parallelism</td>
</tr>
<tr>
<td>Exploits thread and instruction level</td>
<td>SMP (Symmetric MP)</td>
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<table>
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<tr>
<th>Latency-limited</th>
<th>SMP (Symmetric MP)</th>
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<tr>
<td>Only exploits program level Parallelism</td>
<td>SMP (Symmetric MP)</td>
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<table>
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<tr>
<th>Still limited by memory latency</th>
<th>Multiple Processes</th>
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<tbody>
<tr>
<td>Difficult to program/debug</td>
<td></td>
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<table>
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<tr>
<th>Little help with network traffic</th>
<th>Faster, larger caches</th>
</tr>
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<tr>
<td>Doesn't help latency problem</td>
<td>Wider memory</td>
</tr>
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</table>

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<tr>
<th>Faster clock = Longer stalls</th>
<th>Faster clock</th>
</tr>
</thead>
<tbody>
<tr>
<td>Benefit is Latency-limited</td>
<td>Solution</td>
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</table>

**Status**

**Solution**

**Alternative Solutions**

**Networks**

**Clearwater**
Up to 10 Gbps throughput:
25 million packets per second forwarding rate at 300 MHz:

- Reference Evaluation Kit
  (on-chip ICE)
- Advanced Debug Capability
- Standard Interfaces
- Development Tools
- Standard Software
- Runs MIPS-compatible
- Ease of Design

Enhancements:
- Architectural Performance
- High Bandwidth Interfaces
- SMICore

High Performance Processor

Network Services Processor

Our Solution: The CN810SP
Major Blocks:

System Interface

XpressTM Switch

Packetcache

On-chip

Management

Packet

unit (PMU)

unit (SPU)

unit (SIU)

CNP8105SP™ Network Service Processor
CN8410™ SMT Core

- 8 Simultaneous Threads
- 8 Instruction Queues
- 8 Sets of Registers
- Up to 8 packets at a time
- 10 Functional Units
- Issues up to 8 instructions
- and 2 Load/Stores
- WMU: 64-entry TLB
- runs MIPS-compatible
- NPX™ Extensions
code
- instruction and
- instruction set
- 4-way
- Caches
- 64 KB each
CNP810SP \( \geq 25 \text{ MPPS forwarding rate at } 300 \text{ MHZ} \)

- Ideal for packet processing
- Hides memory latency

SMT is more efficient than SMP
- Used to accelerate TCP checksum
- One's complement add & subtract
- Programmer-defined masks
- Simplices header traversal by allowing up to 32 bytes to be loaded
- LDX/STX - masked load/store instructions
- NPX Examples
- 3rd Party tool chain provides NPX support
- Advantage
- Not required, but they can provide additional performance
- Additional instructions to accelerate packet processing
- Network Processing Extensions - a small number (~10) of

What are NPX™?
24 global and 8 per thread masks
- Allows efficient key extraction
- Reduces load/store operations by pre-loading registers
- Prioritized packet processing
- Hardware-based management of order of arrival of queues and
  Offload packet I/O operations from SMT core

Packet Management Unit Coprocessor
PacketCache can also be configured as on-chip scatter-gather DMA engines. Additional packets managed in DRAM via advanced growth and packet growth allows efficient packet manipulations including header packet-based memory allocation. Peak data transfers of 9.6 GBytes/second — Fully pipelined — Dual ported (2 simultaneous reads & writes) — 16-byte line with byte enables 256 KB Packet Memory

On-chip PacketCache™
- 133 MHz, 64-bit PCI-X (8.3 Gbps peak)
- 3.2 Gbps each
- Single, full-duplex SPI-4 (12.8 Gbps) or dual full-duplex SPI-3

Standard Interfaces

- Peak on-chip bandwidth of 225 Gbps
- Four high-performance DMA engines
- Point-to-point (not shared)

On-chip XPress Switch™

- Memory streaming across channels for optimized utilization
- 16 banks (4 32-bit channels, 4 banks per channel)
- Peak 75 Gbps data transfer
- 300 MHz (600 MHz data) DDR SDRAM

High Performance Memory Subsystem

High Performance Interfaces
- Minimal contention
- Optimized for packet movement
- Industry leading performance
- High bandwidth external memory subsystem

- Multi-purpose memory
- Optimized for header and packet manipulation
- High speed managed memory

- ON-Chip PacketCache™
- Better resource utilization
- Prevents starvation of functional resources
- Simultaneous Multi-threading

Latency Bottleneck
Key Features to Solve the Memory

Clearwater Networks
and performance profiling

Unique visibility into the entire system for software development

- Architectural state
  • Read & write all architectural state
  • Threads simultaneously
  • Supports trace on up to 2 state with time stamps
  • Full real-time execution
  • Execution Trace
  • Breakpoints
  • Hardware Execution
  • Halt/Go individual threads
  • Run Control

On Chip Instrumentation Features

Networks Clearwater
CNP810SP Physical Specifications

- 1.5 microm
- 1312 pin FC BGA
- 1.5V, 2.5V, 8, 3.3V I/O
- 1.2V core
- 12W typ. @ 300 MHz
CNP810SP System Implementations
Complete Product Suite
Scalable architecture for 10GE, OC-192 and beyond

Simple Programming Model
- High-speed Interfaces
- Memory subsystem
- SMT core

Combination of

Overcomes memory latency bottleneck through a

efficient network services

Specifically designed for implementing advanced

Introducing CNP810 processor family: processors

Summary